

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

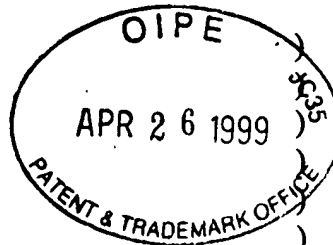
In re Application of

Shigeru ATSUMI

Serial No.: 09/028,276

Filed: February 24, 1998

For: Semiconductor Integrated Circuit
Device and Flash EEPROM



Atty. Docket: 01701.73982

Group Art Unit: 2815

Examiner: J. Fenty

#1

REQUEST FOR APPROVAL OF DRAWING CHANGES

Assistant Commissioner for Patents
Washington, D.C. 20231

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APR 28 1999
TECHNOLOGY CENTER 2800

Sir:

The Examiner's approval is respectfully requested for the proposed changes to the drawings shown in red in the accompanying copy. Specifically, the proposed changes are as follows:

Figure 8, add the marking to transistor P1 to show that it is a PMOS transistor.

Figure 11, add the label --TMin--.

Following approval of these changes, a bonded draftsman will be contacted to implement them upon receipt of a Notice of Allowance.

A duplicate copy of this paper, including the accompanying copy of the drawings, is included.

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APR 28 1999

Respectfully submitted,

TECHNOLOGY CENTER 2800

Dated: April 26, 1999

By: Gary D. Fedorovich #35,509
for Joseph M. Potenza
Registration No. 28,175

Banner & Witcoff, Ltd.
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1001 G Street, N.W.
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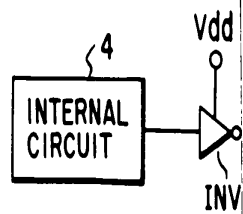


FIG. 10

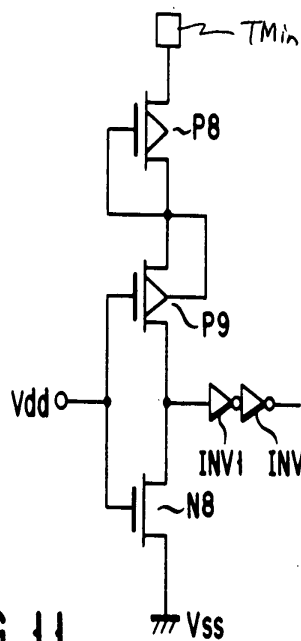


FIG. 11



FIG. 12

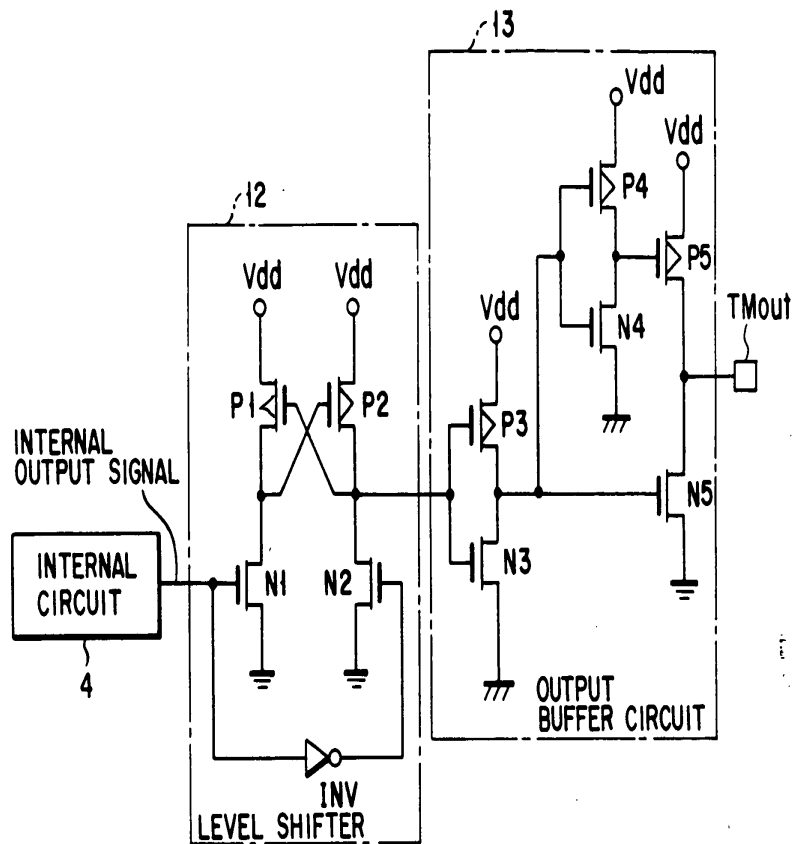


FIG. 8

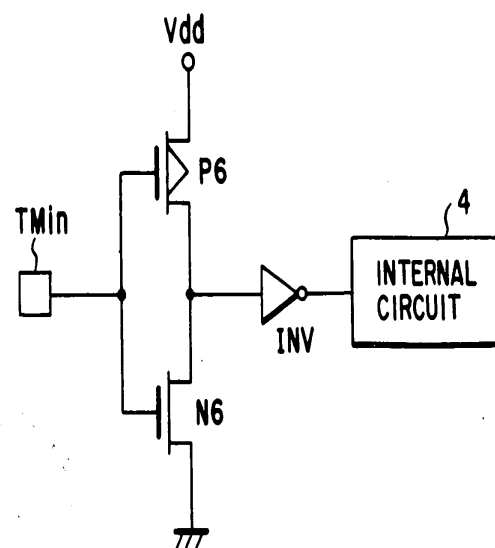


FIG. 9

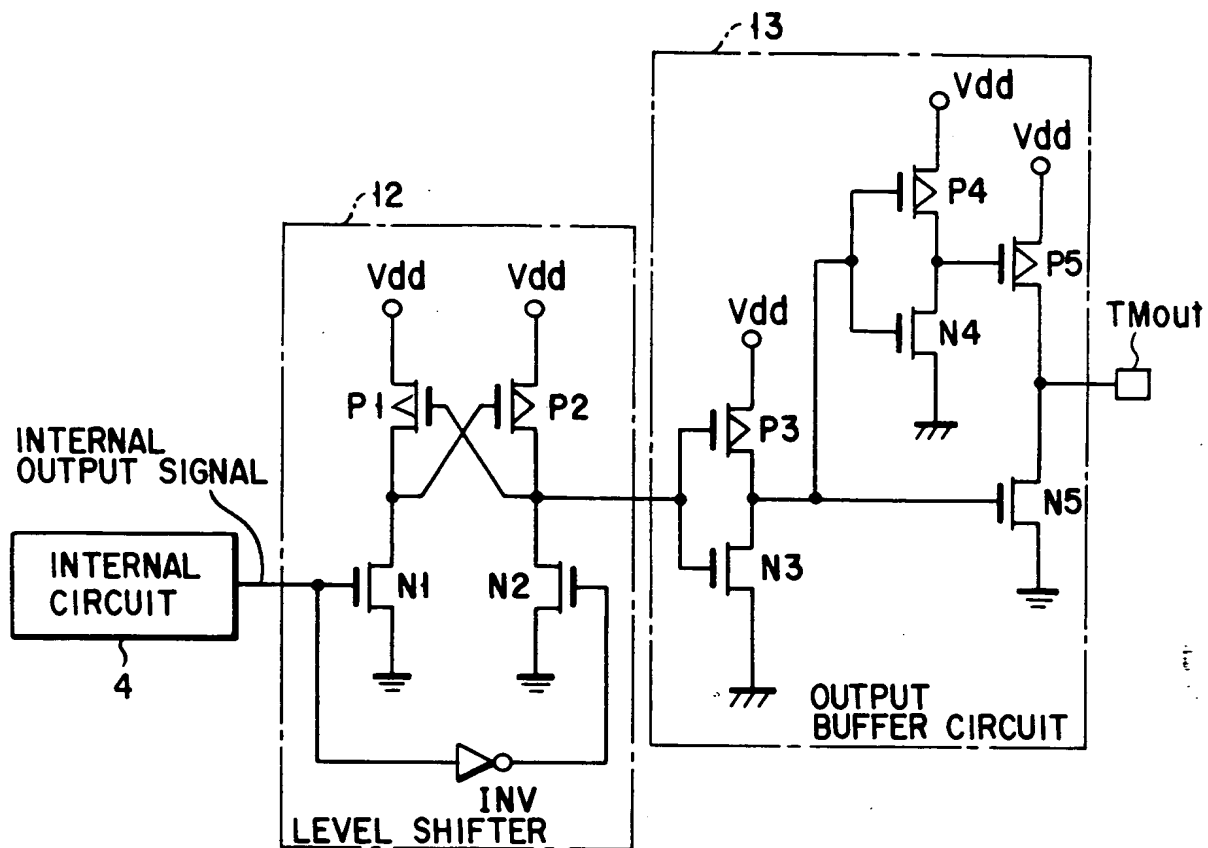


FIG. 8

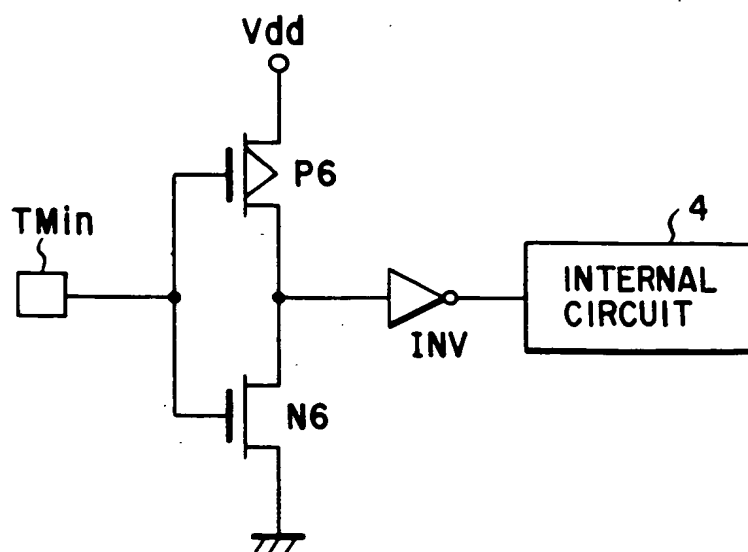


FIG. 9

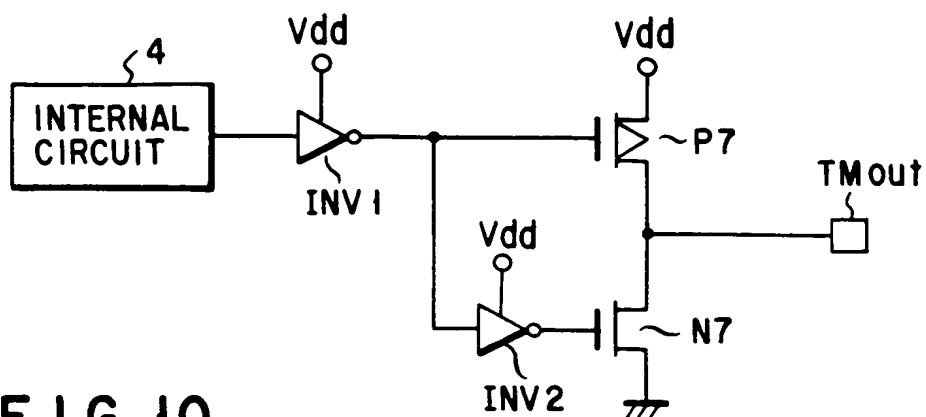


FIG. 10

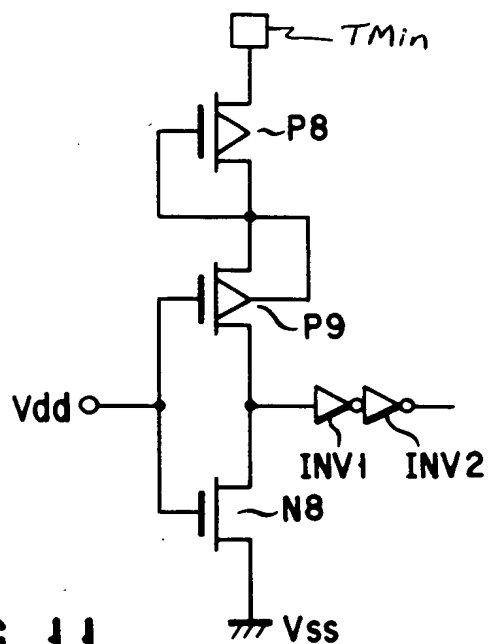


FIG. 11

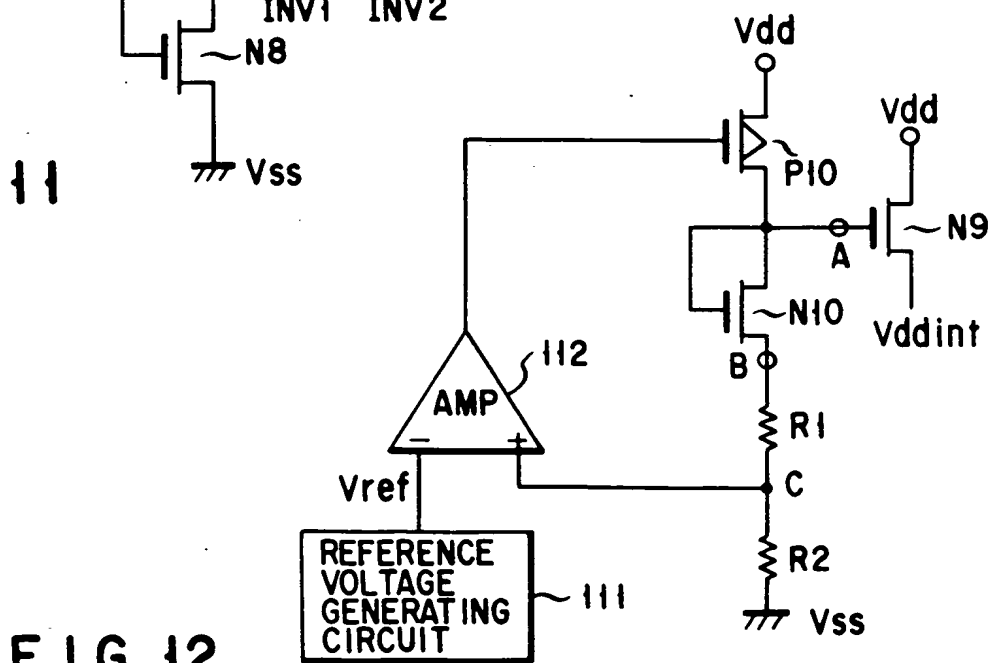


FIG. 12



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